

A

B

C

D

1

2

3

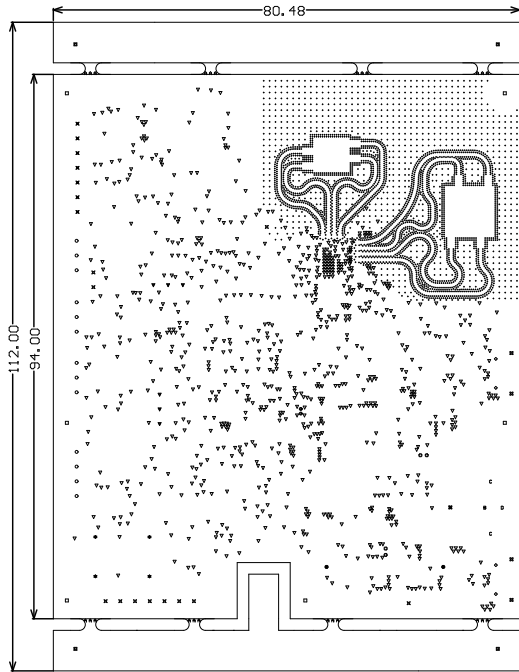
4

5

6

Symbol	Count	Hole Size	Hole Length	Plated	Hole Type	Drill Layer Pair	Hole Tolerance (+)	Hole Tolerance (-)
☆	3453	7.00mil (0.178mm)	-	PTH	Round	Top Layer - L2_GND1	0.00mil (0.000mm)	0.00mil (0.000mm)
⊙	2	7.87mil (0.200mm)	-	PTH	Round	Top Layer - Bottom Layer		
⊕	4	7.87mil (0.200mm)	-	PTH	Round	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)
▽	911	8.00mil (0.203mm)	-	PTH	Round	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)
△	24	19.69mil (0.500mm)	-	NPTH	Round	Top Layer - Bottom Layer		
⊗	4	23.62mil (0.600mm)	51.18mil (1.300mm)	PTH	Slot	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)
◇	4	33.47mil (0.850mm)	-	PTH	Round	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)
★	4	35.43mil (0.900mm)	-	NPTH	Round	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)
B	1	39.37mil (1.000mm)	90.55mil (2.300mm)	PTH	Rectangle	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)
C	2	39.37mil (1.000mm)	98.43mil (2.500mm)	PTH	Rectangle	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)
⊗	1	39.37mil (1.000mm)	118.11mil (3.000mm)	PTH	Rectangle	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)
⊗	11	40.00mil (1.016mm)	-	PTH	Round	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)
⊕	2	40.16mil (1.020mm)	-	NPTH	Round	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)
⊗	7	40.16mil (1.020mm)	-	PTH	Round	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)
○	13	43.31mil (1.100mm)	-	PTH	Round	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)
▽	6	45.28mil (1.150mm)	-	PTH	Round	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)
D	1	62.99mil (1.600mm)	-	NPTH	Round	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)
□	6	118.11mil (3.000mm)	-	PTH	Round	Top Layer - Bottom Layer	3.00mil (0.076mm)	3.00mil (0.076mm)
■	4	160.00mil (4.064mm)	-	NPTH	Round	Top Layer - Bottom Layer	2.00mil (0.051mm)	2.00mil (0.051mm)
4460 Total								

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout



NOTES:

- BOARD SHALL MEET THE REQUIREMENTS OF UL-796E WITH FLAMMABILITY RATING OF MINIMUM 94V-0. UL LOGO, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE RENDERED IN SILKSCREEN.
- VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED, PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED "VIA TENTING/COVERING" REQUIREMENTS.
- MANUFACTURER'S IDENTIFICATION, DATE CODE LETTER SHALL BE SILKSCREENED ON SOLDER SIDE OF THE BOARD.
- TRACE WIDTH SHOULD BE ACCURATELY ETCHED. MAX TOLERANCE +/- 1 MIL.
- LAYER TO LAYER REGISTRATION SHALL BE WITHIN +/- 2 MIL.
- REFER IMPEDANCE TABLE FOR IMPEDANCE CONTROL TRACES ON LAYER 1, 3, 6 & 8.
- FOR ACCURACY OF THE ANTENNA DIMENSION, NEED TO BE MEASURE THE ANTENNA DIMENSIONS ON ONE BOARD.
- ALL VIAS ARE TENTED ON BOTH SIDES UNLESS OTHERWISE SOLDER MASK OPENED IN GERBER.
- VIA HOLE OFFSET SHALL BE WITHIN 1MILS OF ITS ORIGINAL LOCATION
- 7 MIL VIA SHOULD BE FILLED WITH CONDUCTIVE COPPER AND SURFACE SHOULD BE FLAT
- BGA AREA VIAS SHOULD BE CAPPED WITH COPPER PLATING TO ENSURE FLAT SURFACE
- FLATNESS TOLERANCE FOR VIA ON PADS: +0.000 /- 0.001 INCHES ON BOTH SIDES.

LAYER STACK-UP :

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.80mil	1	
1	Top Layer		1.60mil		
	Dielectric 1	R03003	5.00mil	3	
2	L2_GND1		1.40mil		
	Dielectric 2	PCL370HR	5.50mil	3.9	
3	L3_SIG1		1.40mil		
	Dielectric 3	PCL370HR	10.00mil	4.25	
4	L4_PWR1		1.40mil		
	Dielectric 4	PCL370HR	5.50mil	3.9	
5	L5_PWR2		1.40mil		
	Dielectric 5	PCL370HR	10.00mil	4.25	
6	L6_SIG2		1.40mil		
	Dielectric 6	PCL370HR	5.50mil	3.9	
7	L7_GND2		1.40mil		
	Dielectric 7	PCL370HR	5.00mil	4.25	
8	Bottom Layer		1.60mil		
	Bottom Solder	Solder Resist	0.80mil	1	
	Bottom Overlay				

NOTE :

- THIS IS AN IMPEDANCE CONTROLLED BOARD.
- EXTERNAL LAYER CU THICKNESSES ARE FINISHED THICKNESS AFTER PLATING.

IMPEDANCE TABLE : 6

LAYER	TRACE WIDTH	SPACING	IMPEDANCE +/- 10%	REFERENCE LAYER
TOP	8.386 MILS	3.944 MILS	50 OHM	LAYER-2 (GND LAYER)

LAYER	TRACE WIDTH	SPACING	IMPEDANCE +/- 10%	REFERENCE LAYER
TOP	10.8 MILS	-	50 OHM	LAYER-2
BOTTOM	8.7 MILS	-	50 OHM	LAYER-7
L3 & L6	6 MILS	-	50 OHM	LAYER-2, LAYER 7
TOP	7.5 MILS	4 MILS	90 OHM	LAYER-2
BOTTOM	6 MILS	5 MILS	90 OHM	LAYER-7
L3	5 MILS	5.9 MILS	90 OHM	LAYER-2, LAYER 4
TOP	4.3 MILS	5.5 MILS	120 OHM	LAYER-2
TOP	5.8 MILS	4.2 MILS	100 OHM	LAYER-2
BOTTOM	5.9 MILS	3.9 MILS	100 OHM	LAYER-7
L3	4.8 MILS	7.2 MILS	100 OHM	LAYER-2, LAYER 4

DESIGN INFORMATION

MIN. TRACK WIDTH: 4.8 MIL
MIN. CLEARANCE: 3.9 MIL
MIN. VIA PAD SIZE: 13.72 MIL
MINIMUM ANNULAR RING 0.127mm (5.0MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

☐ FR-408 ☐ FR-4 High Tg ☒ OTHER REFER STACK-UP

THICKNESS: ☐ 62 MIL (1.6mm) +/-10% ☒ OTHER 59 MIL +/-10%

TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2

☐ OTHER +/-

BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2

☐ OTHER +/-

DRILLING:

REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES

PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER

BOARD FINISH:

SILKSCREEN: ☒ TOP ☒ BOTTOM

SILKSCREEN COLOR: ☒ WHITE ☐ OTHER

SOLDER RESIST COLOR: ☐ GREEN ☒ OTHER RED

☐ MATTE ☒ SEMI-GLOSS

SURFACE FINISH: ☐ IMMERSION GOLD (ENIG) ☐ ENEPIG

☐ IMM. TIN/SILVER OR EQUIV ☒ OTHER IMM. SILVER

ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE

☒ N.C. ROUTE ☐ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs

TO MEET OR EXCEED THE REQUIREMENTS OF:

☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3

☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: ☐ YES

BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER

☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

☐ LAYER 1 & 6 (INNER LAYERS) XX MIL WIDE, 59 MIL SPACE

TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PROJECT TITLE:
xJRL6844 EVM

DESIGNED FOR:
Public Release

FILE NAME:
PROC182A_PCB.PcbDoc

ENGINEER:
Mistral

LAYOUT BY:
Mistral

SCALE: 1.00

ALTUM DESIGNER VERSION:
22.11.1.43

ALL ARTWORK VIEWED FROM TOP SIDE

BOARD #: PROC182

REV: A

SUN REV: 4094 [Modified]

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LAYER NAME = Hi Board Outline
Fabrication Dimensions

TID #: N/A

PLOT NAME = Fabrication Drawing 1

GENERATED : 20-11-2024 14:25:53

TEXAS INSTRUMENTS

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